1. For the circuit shown in Figure 1, utilize the constant-voltage-drop model (0.5V) for each conducting diode, please draw the v_i-v_o transfer characteristic plot. [10 分]

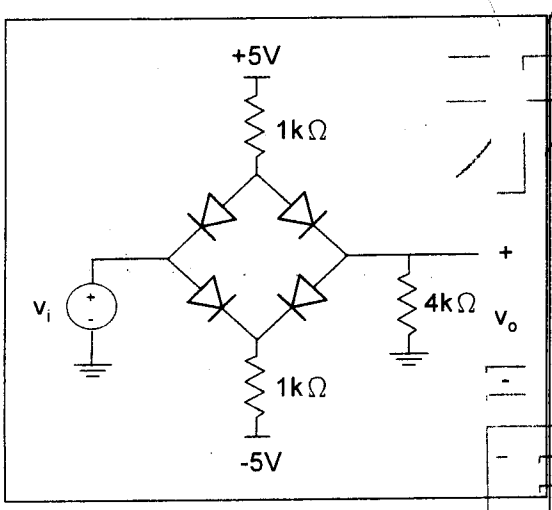


Figure 1

```
* CMOS Amplifier
Vdd   1   0   DC   +10V
Iref  2   0   DC   100uA
Vi    4   0   DC   0V
M1    3   4   0   0   nmos   L=10u W=100u
M2    3   2   1   1   pmos   L=10u W=100u
M3    2   2   1   1   pmos   L=10u W=100u
.model   nmos   nmos(kp=20u Vto=+1V lambda=0.01)
.model   pmos   pmos(kp=10u Vto=-1V lambda=0.01)
.DC   Vi   0V   +10V   10mV
.PLOT   DC   V(3)
.probe
.end
```

Figure 2

2. For the SPICE netlist shown in Figure 2. (a) Please redraw its circuit. (b) Find the small-signal voltage gain. (c) Also draw its v_i-v_o transfer characteristic plot, please label the proper operation modes of transistors in the plot.(kp = k' : process transconductance, Vto : zero-bias threshold voltage, lambda = λ = V_A^{-1} : channel length modulation)

[(a) 5 分 (b) 7 分 (c) 8 分]

3. For the circuit shown in Figure 3, neglect base currents and use the exponential i_C-v_{BE} relationship to show that

$$I_b = I_{ref}\sqrt{\frac{I_{S3}\, I_{S4}}{I_{S1}\, I_{S2}}}$$

(I_S is the transistor's saturation current)

[10 分]

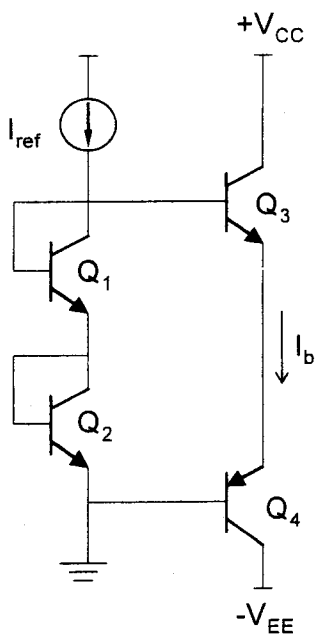


Figure 3

4. Assuming the op amp to be ideal, (a) please derive the close-loop gain v_O/v_I of the circuit shown in Figure 4. (b) Use this circuit to design an inverting amplifier with a gain of 100 and an input resistance of 1MΩ. Assume that for practical reasons it is required not to use resistors greater than 1MΩ. [(a) 10 分 (b) 10 分]

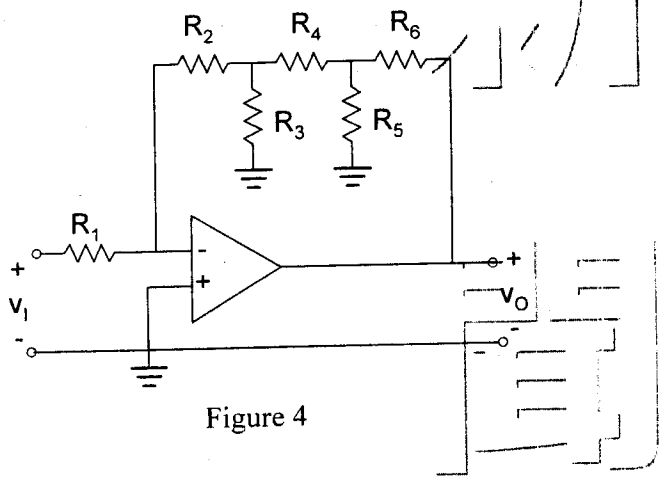


Figure 4

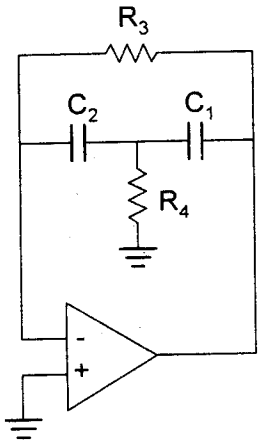


Figure 5

5. Assuming the op amp to be ideal, (a) please derive the open-circuit voltage transfer function of the RC network shown in Figure 5. (b) If R1=R2=R and C1=C2=C, and denote CR=τ, please find the poles of the closed-loop amplifier. [(a) 10 分 (b) 10 分]

6. For the amplifier shown in Figure 6, uses transistors with β=100, please evaluate the following:

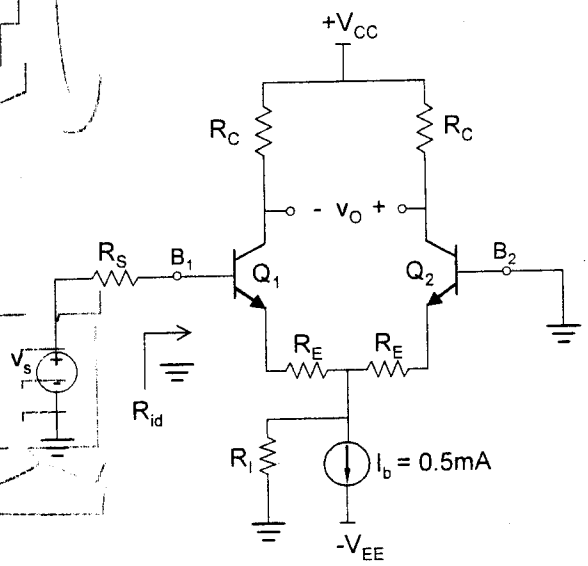
(a) The input differential resistance R_{id}.

(b) The overall voltage gain v_o/v_s (neglect the effect of r_o).

(c) The worst-case common-mode gain if the two R_Cs are accurate to within ±2%.

(d) The CMRR, in dB. (log2 = 0.3)

[(a) 5 分 (b) 5 分 (c) 5 分 (d) 5 分]



(R_C=10kΩ, R_S=10kΩ, R_E=50Ω, R_I=200kΩ) Figure 6